Class-B Power MMIC Amplifiers with 70 Percent Power-Added Efficiency

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Abstract — *C*-band monolithic amplifiers using high-efficiency, class-B MSAG processing have been designed, fabricated, and tested. The class-B single-ended amplifier design employed reactive termination for higher order harmonics and achieved state-of-the art efficiency of 70 percent with associated gain of 8 dB and output power of 1.7 W over the 5–6 GHz band.

I. Introduction

THERE IS a great deal of interest in finding efficient, reliable, and low-cost power sources for the T/R modules used in phased array antennas. Many companies have designed high-power MMIC amplifiers in order to meet this challenge. We have developed [1] a single-chip 10 W class-A power MMIC amplifier demonstrating state-of-the-art performance with 5 dB gain and 36 percent power-added efficiency at 5.5 GHz. We also achieved 17 W power out, 4.5 dB gain with 32 percent power-added efficiency, by combining these two chips using external combiners.

However, the need to reduce prime power and cooling requirements for large antenna arrays puts a tremendous premium on achieving significantly higher power-added efficiency. Accordingly, we have investigated class-B amplifiers which have the following potential advantages compared to class A:

- Higher power-added efficiency.
- Negligible power dissipation at no RF power.
- Under backoff, the efficiency of the class-B amplifier does not degrade as rapidly as that of the class-A amplifier.
- A dynamic range of about 10 dB over which the power-added efficiency is greater than 40 percent and the gain is almost constant.

High-efficiency hybrid class-B power amplifiers have been reported in the literature [2]–[9]. Power-added efficiency (*PAE*) of 45 percent with associated gain of 5.4 dB over the 9.2–10.2 GHz band was achieved for a 2 W push–pull power amplifier [5]. For harmonic reaction amplifiers the *PAE* obtained was 75 percent with 2.7 W output power and 9 dB gain at 1.7 GHz [6], while a 5 W amplifier demonstrated 70 percent *PAE* with 9 dB gain at 2 GHz [7]. An *X*-band power amplifier using a harmonic tuning technique has achieved 5 W of output power with 6 dB gain and 36 percent *PAE* at 10 GHz [8]. A quasi-monolithic 4 GHz power amplifier has demonstrated 65 percent *PAE*, 1 W power output, and 10 dB gain [10].

This paper describes the design, fabrication, and test results of a fully monolithic class-B power amplifier with 70 percent *PAE* at *C*-band. In addition to discussing power output, gain, and *PAE* as a function of input power, drain–source voltage, and gate–source voltage, this paper includes data on noise figure, AM to PM conversion, and second- and third-harmonic generation.

II. Models for Class-B Power FET's

The FET used in our class-B power amplifiers has a 2.5 mm gate periphery. This device employs two plated-through source vias for low-inductance source grounding and good heat sinking. The FET's are biased near pinch-off at a drain–source current of 5 percent I_{DSS} and a drain–source voltage of 12 V.

An innovative method has been developed at the ITT Gallium Arsenide Technology Center (GTC) to determine accurate linear-type models for class-B power FET's which are used to design MMIC power amplifiers. A similar technique has been employed successfully at GTC to design class-A power MMIC amplifiers [1]. The model is derived from I–V characteristics, small-signal S parameters measured at 5, 25, and 50 percent of I_{DSS}, and load-pull contour data at the operating drain–source voltage and frequencies. An equivalent lumped-element model for the 2.5 mm FET biased at $V_{DS} = 12$ V is shown in Fig. 1. This model is directly used to design matching networks for maximum efficiency of an MMIC amplifier operating in class-B mode.

III. 1.5 W Power Amplifier Design

The push–pull configuration has been extensively used for class-B power amplifiers at low frequencies. However, at microwave frequencies low-loss transformers (baluns) for push–pull amplifiers are required to cancel the second harmonic, which is generated when the FET's are biased near pinch-off. Because power MMIC amplifiers must be

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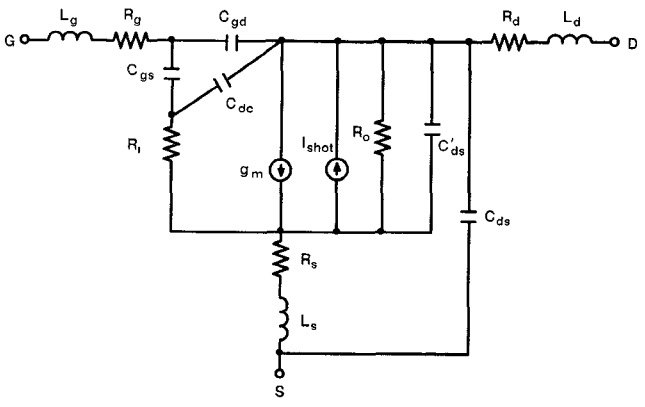

$R_g = 2\ \Omega$ $C_{gs} = 2.5$ pF
$R_i = 0.4\ \Omega$ $C_{gd} = 0.1$ pF
$R_s = 0.6\ \Omega$ $C_{ds} = 0.05$ pF
$R_d = 0.3\ \Omega$ $C'_{ds} = 0.1$ pF
$R_o = 70\ \Omega$ $C_{dc} = 0.1$ pF

$L_g = 0.05$ nH $g_m = 150$ mS
$L_s = 0.08$ nH $I_{shot} = 0.8$
$L_d = 0.07$ nH

Fig. 1. Lumped-element model for a 2.5 mm class-B power FET.

fabricated on very thin substrates for good thermal dissipation, it is almost impossible to realize these transformers with less than 1 dB insertion loss, since the component loss is inversely proportional to substrate thickness. A transformer with 1 dB loss will lower the *PAE* of a push–pull amplifier by 20 percent. Therefore, the push–pull configuration was not utilized for narrow-band power amplifier designs for our high-efficiency applications. Keeping in mind all the possible limitations, we selected a single-ended class-B amplifier design.

The single-ended class-B amplifier design consists of the reactive termination of higher order harmonics. Two RF bypass capacitor terminated short-circuited stubs ($\lambda/4$ and $\lambda/6$ at band center frequency) connected at the drain location reactively short the second and third harmonics to increase the overall efficiency of the circuit [10], [11]. The short-circuited quarter-wavelength stub does not affect the fundamental frequency performance. However, at twice the fundamental frequency, the line becomes $\lambda/2$ long, providing low impedance to the second harmonic. The short-circuited $\lambda/6$ stub is inductive at the fundamental frequency and is part of the matching network. At three times the fundamental frequency, this line becomes $\lambda/2$ and reactively terminates the third-harmonic component.

The 1.5 W power class-B MMIC design is based on the design methodology developed at ITT/GTC. The 2.5 mm FET (Fig. 1) for maximum efficiency is matched to 50 Ω input and output. Both distributed and lumped elements were used in the matching networks. The elements of the output matching network were selected for minimum possible loss with a good match as well as to satisfy electromigration requirements (maximum allowed current density in the bias lines was 2×10^5 A/cm^2). Capacitors, which were used for dc blocking, RF bypassing, and matching, were all of the metal–insulator–metal (MIM) type. The dielectric material used for the capacitors is 2000-Å-thick Si_3N_4.

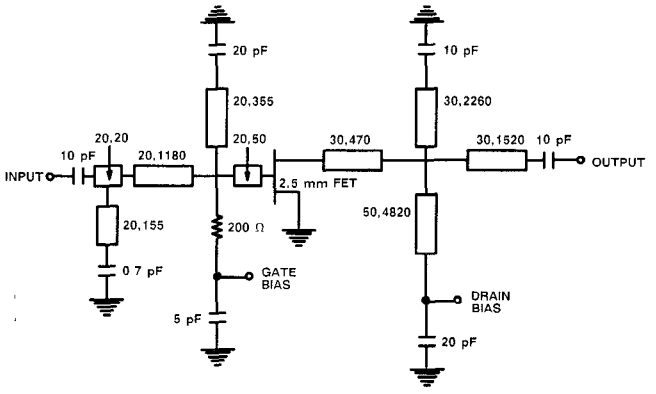

Fig. 2. Schematic of 1.5 W class-B MMIC amplifier. All dimensions in μm.

This provides a capacitance of 300 pF/mm^2 and a breakdown voltage above 30 V. The tolerance in capacitance is ±5 percent. Large RF bypass capacitors as well as resistive gate bias were used for amplifier stabilization at low frequency. The drain bias is applied through a short-circuited stub which is also a part of the output matching network. The amplifier design was optimized over the 5–6 GHz frequency. A schematic of the amplifier is shown in Fig. 2.

IV. Fabrication

The class-B power IC's reported in this paper are fabricated using the refractory metal, multifunctional self-aligned gate (MSAG) MMIC process developed at ITT/GTC. The process flow diagram is shown in Fig. 3 and a detailed description of the process is given in [12]. Some of the key features of the process are as follows:

- Since the FET I_{DSS} is determined by implantation rather than gate recess, I_{DSS} uniformity is remarkably improved. Typical uniformity is better than 5 percent.
- Gate–source resistance is minimized using an n^+ implant which aligns itself to the gate. FET performance is reasonably insensitive to gate location, resulting in excellent photolithography tolerance.
- The Schottky metal is titanium–nitride (TiWN), an extremely good gold diffusion barrier. Given that the Schottky survives an 825°C anneal, it is unlikely to fail at less than 300°C.
- The gate parasitic resistance is reduced to a very low level using gold overlay metal which is isolated from the GaAs surface by silicon nitride dielectric and the TiWN Schottky.
- The n^+ on the drain side is moved away from the gate to maintain high gate–drain breakdown voltage and high output resistance.

The devices reported here employ coimplantation of n-type (Si) and p-type (Mg) impurity ions in their active regions. This was done in order to increase the FET transconductance, especially near pinch-off bias, by increasing the abruptness of the charge density profile, and to increase carrier confinement, and hence breakdown

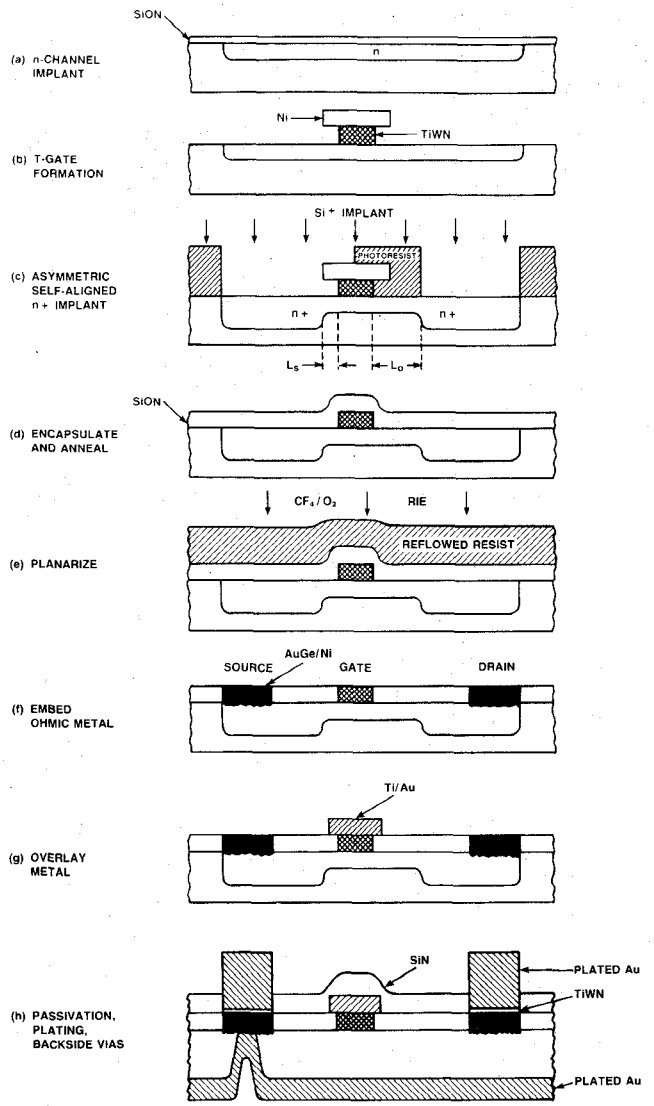

Fig. 3. MSAG FET fabrication process flow diagram.

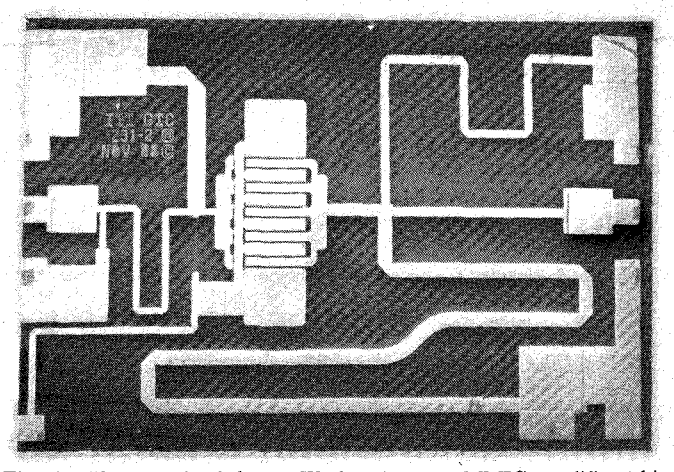

Fig. 4. Photograph of the 1.5 W class-B power MMIC amplifier (chip size = 4.8 mm^2).

voltage, by generating a p–n junction at the channel–substrate interface.

The process includes Au/Ge/Ni metallization for ohmic contacts, 0.5 μm TiWN Schottky barrier gates, and ion-implanted resistors. The 0.5 μm TiWN gates are covered by a 0.8 μm overlay after planarization. Silicon nitride is used for both capacitors and passivation. The air bridges, microstrip lines, and bonding pads are 5-μm-thick plated gold. The wafer is lapped to its final thickness of 75 μm, and back side via holes are then etched and plated. A photograph of the chip is shown in Fig. 4. The measured functional on-wafer yield for four wafers in a lot is plotted in Fig. 5. (This is a low-power screening test.)

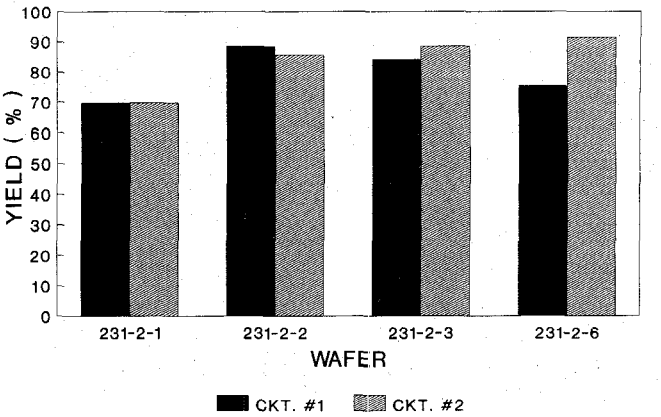

Fig. 5. Functional yield of 1.5 W class-B power MMIC amplifier from a lot of four wafers.

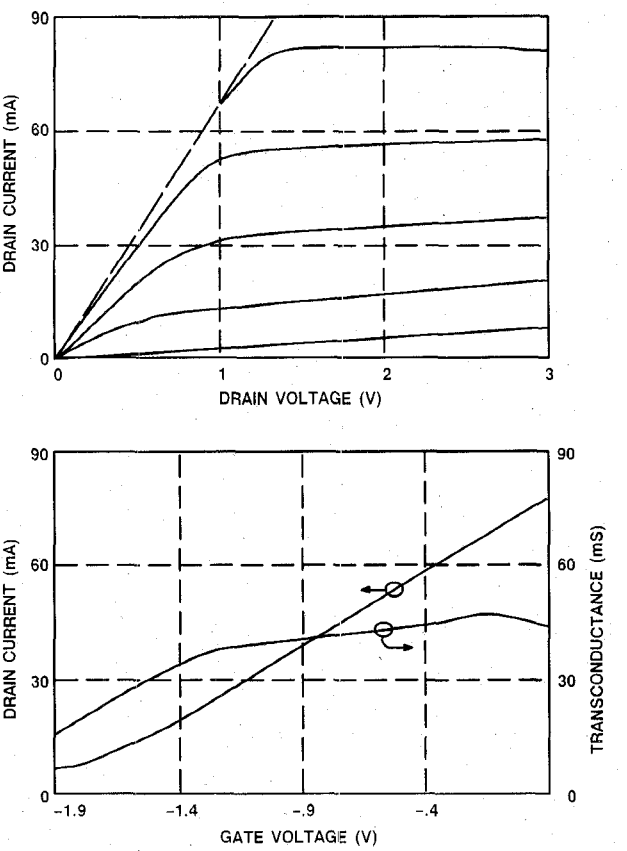

Fig. 6. Typical measured dc data for a 300 μm class-B power FET.

V. Test Results

Fig. 6 shows the dc characteristics of a 300 μm FET tested on the wafer. The typical I_{DSS} is 80 mA, and the pinch-off voltage is -2 V. At pinch-off the gate–drain breakdown voltage (defined as $I_{GD} > 1$ mA/mm) is

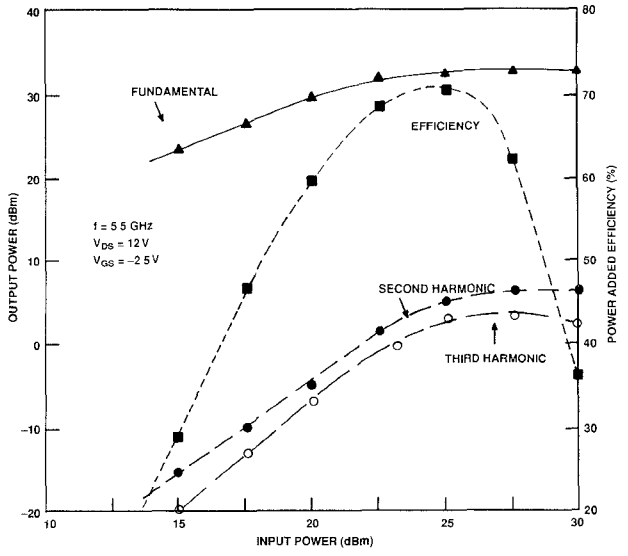

Fig. 7. Output power for fundamental, second and third harmonic and power added efficiency versus input power of a 1.5 W class-B MMIC amplifier.

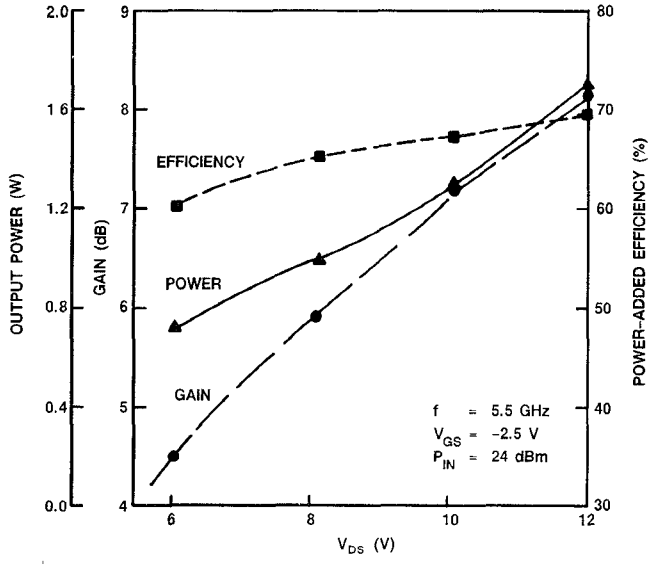

Fig 8. Power output, gain, and efficiency versus drain–source voltage

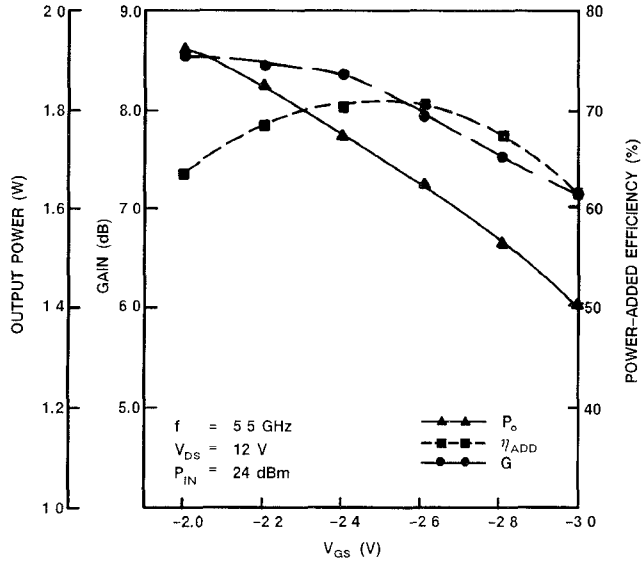

Fig. 9 Power output, gain, and efficiency versus gate–source voltage

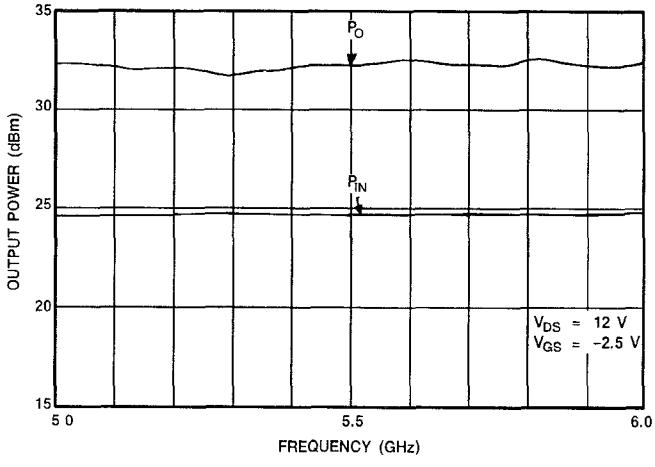

Fig 10 Variation of power output and power input as a function of frequency over the design frequency range

approximately 23 V. At half I_{DSS}, the dc transconductance is 40 mS (133 mS/mm).

Several 1.5 W amplifiers were assembled on 0.5×0.5 in^2 Elkonite (Cu–W) carriers. Elkonite material (a standard material for MMIC packages as well as for carriers at GTC) was chosen for its good thermal conductivity and good thermal expansion match to GaAs and alumina.

Typical measured characteristics for the IC are plotted in Fig. 7 as a function of input power at 5.5 GHz (center frequency of the 5–6 GHz design band). The amplifier has about 1.7 W power output, 8 dB gain, and 70 percent *PAE*. The second- and third-harmonic levels were below −26 dBc and −28 dBc, respectively. Figs. 8 and 9 depict power output, gain, and efficiency as functions of V_{DS} and V_{GS}, respectively. These plots show that GTC's class-B amplifier chips exhibit more than 60 percent *PAE* over a large range of bias voltages. At maximum efficiency, power output and input power as a function of frequency are shown in Fig. 10. The variations of input and output return loss are plotted in Fig. 11. Over the design band the return loss was better than 10 dB. The measured group delay of the amplifier was 0.2 ns.

The noise figure of the class-B amplifier was measured when biased at 20 percent of I_{DSS}. Noise figure and small-signal gain as a function of frequency are plotted in Fig. 12. The noise figure was less than 3.5 dB over the 5–6 GHz band. Also, the spectrum of a frequency synthesizer signal and the amplified signal by the class-B power amplifier chip were measured and are shown in Fig. 13. It may be noted that the phase noise contribution by the amplifier is negligible. The measured AM to PM conversion was less than 1°/dB up to 20 dBm input power and less than 3°/dB up to 25 dBm input power.

Table I summarizes the measured performance versus design goals for GTC's class-B power amplifiers. At GTC we have demonstrated state-of-the-art performance for

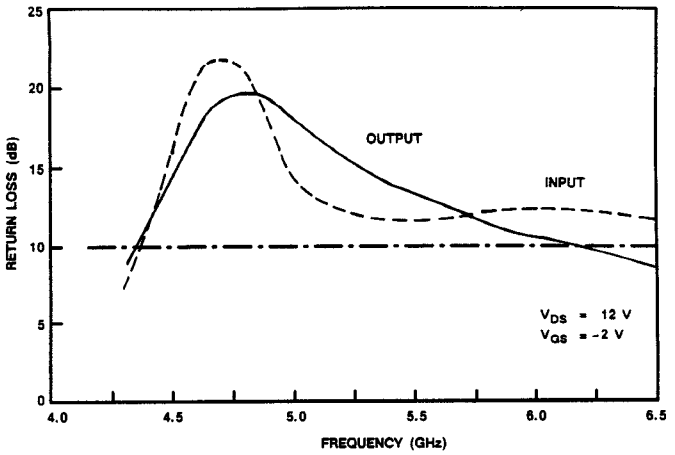

Fig. 11. Return loss versus frequency of a 1.5 W class-B power MMIC chip.

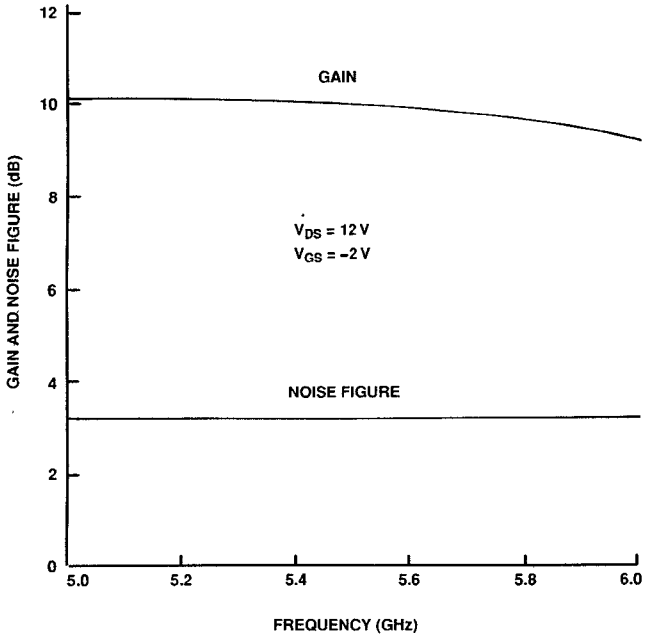

Fig. 12. Typical small-signal gain and noise figure of a 1.5 W class-B MMIC amplifier.

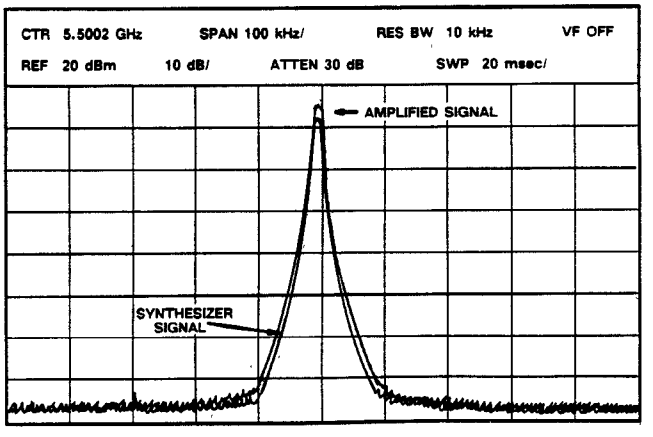

Fig. 13. Spectrum of a frequency synthesizer signal and amplified signal by a class-B amplifier (V_{DS} = 10 V, V_{GS} = −2.0 V, attenuator value = 6 dB).

TABLE I
SUMMARY OF MEASURED RESULTS FOR CLASS B MMIC AMPLIFIERS

Parameter	Goals	Measured
Frequency (GHz)	5-6	5-6
Power Output (W), min.	1.5	1.7
P_o/mm (W/mm)	0.6	0.7
Gain (dB), min.	8.0	8.0
Efficiency (%), min.	50	70
VSWR, Max.	2:1	2:1
IInd Harmonic level (dBc), max.	-20	-26
IIIrd Harmonic level (dBc), max.	-20	-28

class-B power amplifier MMIC's. This excellent performance is attributed to a new IC design method, simple circuit topology, second- and third-harmonic termination at the drain location, and high-yield, high-performance MSAG processing.

VI. Conclusions

A fully monolithic *C*-band class-B power amplifier with 70 percent *PAE*, 8 dB gain, and 1.7 W power output fabricated using the ITT MSAG process (refractory self-aligned gate technology) is demonstrated. The IC's exhibited excellent performance, including −26 and −28 dBc second- and third-harmonic levels at the maximum efficiency, clearly demonstrating the importance of careful harmonic termination.

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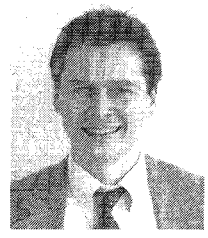
Edward L. Griffin (M'76) was born in Philadelphia, PA, in 1947. He obtained the B.S. degree in engineering physics in 1969, the M.S. degree in physics in 1971, and the Ph.D. degree in solid-state physics in 1975, all from the University of Illinois. In 1988, he was awarded an M.B.A. from Duke University.

He joined the ITT Gallium Arsenide Technology Center in February 1982. Prior to joining ITT, he worked for seven years at Hughes Aircraft Space and Communications Group on the development of a variety of active and passive microwave components for satellite applications. Areas in which he concentrated included microwave filters, CAD and numerical analysis, design manufacturing of low noise and power GaAs FET hybrid amplifiers, and reliability testing. Prior to becoming Director of Engineering, he served as Manager of the GTC MMIC Design and Test Department for three years, followed by two years as Manager of the GaAs IC Fabrication Department. As Director of Engineering at GTC, he has been involved with all aspects of GaAs IC design with all packaging, and testing. He became Director of Engineering/Operations in 1988.

Dr. Griffin served on the IEEE MTT-S Microwave Filter Steering Committee from 1981 to 1983 and the IEEE MTT-S Low-Noise Techniques Technical Committee in 1985. He is the author or coauthor of more than 15 technical papers and is the coholder of six microwave patents. Dr. Griffin is a member of the American Physical Society.



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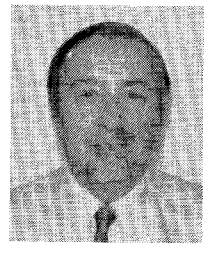

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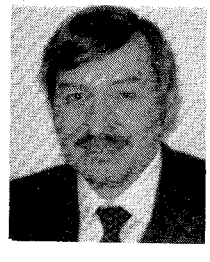

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He joined Hughes Aircraft in 1967, where he was in charge of signal processing and tracking within the Advanced Programs Division. He then became an Associate Manager of the Sensor System Development Department within the F-14 program, which provided the radar hardware and software functional and system design and analysis. Mr. Brukiewa joined ITT Gilfillan in August 1983 and became the Program Manager for the Hybrid Bistatic Radar Manager for Advanced Systems. Since early 1987, he has been the manager of all active array radar programs within ITT Gilfillan, as well as Passive Radar Manager for Advanced Systems. These include the MMIC, power conditioning, variable power T/R module, and in-house IR&D efforts.